

Claims

- [c1] 1. A method of forming a polysilicon layer, comprising the steps of:
- forming an amorphous layer over a panel having a display region and a peripheral circuit region;
 - forming a metallic layer over a portion of the amorphous silicon layer in the peripheral circuit region;
 - performing a crystallization process to transform the amorphous silicon layer in the peripheral circuit region into a first polysilicon layer; and
 - performing an excimer laser annealing operation to transform the first polysilicon layer in the peripheral circuit region into a second polysilicon layer and the amorphous silicon layer in the display region to a third polysilicon layer, wherein the second polysilicon layer has an average grain size greater than the third polysilicon layer.
- [c2] 2. The method of claim 1, wherein the step of forming a metallic layer over a portion of the amorphous silicon layer in the peripheral circuit region comprises:
- forming a mask layer over the amorphous silicon layer, wherein the mask layer has an opening that exposes a

portion of the amorphous silicon layer in the peripheral circuit region; and
forming a metallic layer over the exposed amorphous silicon layer.

- [c3] 3. The method of claim 2, further comprising removing the mask layer.
- [c4] 4. The method of claim 1, wherein the mask layer comprises a silicon oxide layer.
- [c5] 5. The method of claim 1, wherein the metallic layer comprises a nickel layer.
- [c6] 6. The method of claim 1, wherein the step of performing a crystallization process comprises performing a solid-phase crystallization process.
- [c7] 7. The method of claim 1, further comprising forming a buffer layer over the panel with the buffer layer being a stack layer comprising a silicon nitride layer and a silicon oxide layer.
- [c8] 8. A method of fabricating a low temperature polysilicon thin film transistor, comprising the steps of:
forming an amorphous silicon layer over a panel having a display region and a peripheral circuit region;
performing a metal induced crystallization process to

transform the amorphous silicon layer in the peripheral circuit region into a first polysilicon layer;
performing an excimer laser annealing process to transform the second polysilicon layer in the peripheral circuit region into a second polysilicon layer and the amorphous silicon layer in the display region into a third polysilicon layer, wherein the second polysilicon layer has an average grain size larger than the third polysilicon layer;
patterning the second polysilicon layer to form a plurality of island polysilicon layers;
forming a channel region and a doped source/drain region on each side of the channel region in the island polysilicon layers; and
forming a gate over the channel regions.

[c9] 9. The method of claim 8, wherein the step of performing a metal induced crystallization process comprises:
forming a mask layer over the amorphous silicon layer, wherein the mask layer has an opening that exposes a portion of the amorphous silicon layer in the peripheral circuit region;
forming a metallic layer over the exposed amorphous silicon layer; and
performing a crystallization process.

[c10] 10. The method of claim 9, further comprising removing the mask layer.

- [c11] 11. The method of claim 9, wherein the crystallization process comprises a solid-phase crystallization process.
- [c12] 12. The method of claim 9, wherein the mask layer comprises a silicon oxide layer.
- [c13] 13. The method of claim 8, wherein the metallic layer comprises a nickel layer.
- [c14] 14. The method of claim 8, further comprising:
forming a buffer layer over the panel with the buffer layer being a stacked layer comprising a silicon nitride layer and a silicon oxide layer.
- [c15] 15. The method of claim 8, wherein the step of patterning the second polysilicon layer comprises performing a doping operation.
- [c16] 16. The method of claim 11, further comprising forming a gate insulation layer over the island polysilicon layer and the buffer layer.
- [c17] 17. The method of claim 16, wherein the step of forming a channel region and a doped source/drain region on each side of the channel region in each island polysilicon layer comprises:
forming a first patterned photoresist layer over the gate insulation layer to expose the upper surface on each side

of the island polysilicon layer; and
performing a p^+ doping operation.

[c18] 18. The method of claim 17, wherein after the step of performing a p^+ doping operation, further comprises removing the first patterned photoresist layer.

[c19] 19. The method of claim 8, wherein the step of forming a channel region and a doped source/drain region on each side of the channel region in the island polysilicon layers, further comprises:

forming a second patterned photoresist layer over the panel to cover a portion of each island polysilicon layer and expose the upper surface on each side of the island polysilicon layer; and
performing an n^+ doping operation.

[c20] 20. The method of claim 19, further comprising removing the second patterned photoresist layer.

[c21] 21. The method of claim 20, further comprising forming a gate insulation layer over the island polysilicon layers and the buffer layer.

[c22] 22. The method of claim 21, further comprising:
forming a third patterned photoresist layer over the gate insulation layer to expose a portion of each island polysilicon layer close to the doped source/drain region;

and

performing an n^- doping operation.

[c23] 23. The method of claim 22, further comprising removing the third patterned photoresist layer.

[c24] 24. The method of claim 8, further comprising:
forming an inter-layer dielectric over the panel;
forming a plurality of first openings through the inter-layer dielectric and the gate insulation layer to expose the doped source/drain regions; and
forming a plurality of source/drain contact metallic layers so that the source/drain contact metallic layer is electrically connected to the doped source/drain regions through various openings.

[c25] 25. The method of claim 24, further comprising:
forming a passivation layer over the panel; and
forming a second opening in the passivation layer to expose a portion of the source/drain contact metallic layer;
and
forming a pixel electrode over the second opening so that the pixel electrode and the source/drain contact metallic layer are electrically connected through the second opening.

[c26] 26. The method of claim 25, wherein material constitut-

ing the pixel electrode comprises indium–tin oxide.

[c27] 27. The method of claim 25, wherein material constituting the passivation layer comprises silicon nitride.